REMARKS

Section A lists the current status of the claims. Section B addresses the claim rejections in the order in which they appear in the Action of November 29, 2006.

A. Status of the Claims

Claims 1-11 are pending in the application. Claims 1-11were rejected under 35 USC 102(b) as being anticipated by Noguchi, US Patent No. 6,005,270.

B. 35 USC 102(b) Rejections: Claims 1-11

Claims 1-11 were rejected under 35 USC 102(b) as being anticipated by Noguchi.

Claim 1 recites a thin film transistor comprising polysilicon, wherein the polysilicon is formed by a method comprising: depositing a first layer of amorphous silicon; depositing silicon nuclei on the first layer of amorphous silicon; depositing a second layer of amorphous silicon over the first layer and the nuclei, wherein conversion of the first layer to hemispherical grains before deposition of the second layer is substantially prevented; and annealing the first and second layers of amorphous silicon to induce crystallization.

Claim 8 recites a thin film transistor comprising a channel region formed by a method comprising: embedding deposited silicon nuclei between layers of amorphous silicon; and annealing the nuclei and amorphous silicon layers. Claim 5 recites a monolithic three dimensional memory array comprising memory cells, the memory cells comprising polysilicon crystallized by the same method.

For a product-by-process limitation to be granted patentable weight, the product resulting from the process must clearly be different than if the process were not used.

Noguchi teaches a thin film transistor having a polysilicon channel region 31b (Fig. 5d – Fig. 10.) Noguchi teaches to deposit silicon layer 31a as amorphous silicon and to crystallize it using an "ELA process", or Excimer laser anneal (col. 12, line 56 – col. 13, line 14.) Alternatively, in some embodiments, Noguchi teaches crystallizing silicon layer 31b using a conventional solid phase crystallization method (col. 13, lines 12-14.)

Laser annealing of polycrystalline or amorphous silicon is well-known but has disadvantages in that it is difficult to determine and to control the temperature of thin films during laser anneal, and substrates can be thermally damaged by a laser anneal process. Thus the memory of the present invention will be a memory with no substrate damage.

During a laser anneal, a laser beam scans an amorphous film to be crystallized. The silicon crystals grow oriented relative to the path of the laser beam. Silicon crystals grown using the methods described in the present application grow outward from embedded nuclei (see paragraphs [0023], [0031], and [0040] of the present application.) Thus the shape and distribution of silicon crystals making up a polysilicon film will be different in a film crystallized by an ELA process (as in Noguchi) and by the processes described in the present invention.

As the number and orientation of grain boundaries strongly influences carrier mobility, which in turn strongly influences cell behavior, the cell itself will differ significantly. For example, the device channel may be oriented along the direction of laser scan, thus minimizing the number of grain boundaries in the channel, improving mobility and thus improving device performance. Alternatively, the channel can be

oriented at ninety degrees to the direction of laser scan, maximizing the number of grain boundaries in the channel. In the present invention, the silicon nuclei are randomly distributed, and no such preferential orientation is possible.

Noguchi also mentions conventional solid phase crystallization (SPC) as a possible means to crystallize film 31b. As described in the present application, nucleation sites form during SPC, and hemispherical grains tend to form around these nucleation sites, forming a rough, uneven surface (paragraphs [0021]-[0023].) The methods of the present invention prevent such an uneven surface. An uneven surface increases variability across a memory array, which is undesirable. Thus independent claims 1, 5, and 8, and all of their dependent claims, distinguish over Noguchi.

Claim 3 recites the thin film transistor of claim 1, further comprising a charge storage region, wherein the charge storage region is ONO-type. (This summary includes the limitations of claim 3 and claim 2, from which it depends.)

The Examiner points to layer 23a of Fig. 1, describing it as an ONO-type charge storage region, as in claim 3. Applicant respectfully point out that in the embodiment of Fig. 1, charge is stored not in layer 23a, but in floating gate 32a (col. 11, lines 14-18). The function of layer 23a, which is an ONO stacked film, is not storing charge, but rather as in insulating layer (col. 11, lines 3-4), "sealing the charge in the floating gate 32a" (col. 11, lines 16-18.) In contrast, in the embodiment shown in Fig. 8, charge is in fact stored in layer "charge trap insulating film 24a," part of an ONO-type charge storage region, col.14, lines 45-55. Nonetheless claim 3 depends from claim 1 and distinguishes over Noguchi because of the differences in the silicon film making up the channel region, as described for claim 1.

Thus the polysilicon of the memory cells, and the memory array, of the present invention has distinct characteristics because of the method used to crystallize this polysilicon. This different character causes these devices, and this array, to behave differently. Thus claims 1-11 distinguish over Noguchi.

Applicants respectfully request reconsideration.

CONCLUSION

In view of the preceding Remarks, Applicant submits that this application is in condition for allowance. Reconsideration is respectfully requested. If objections remain, Applicant **respectfully requests an interview.** In the event that objections remain, the Examiner is asked to contact the undersigned agent at (408) 869-2921.

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Date

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